What is claimed is:

1. A planar slice of semiconductor substrate material of a first conductivity type provided at one face with a first region of a second conductivity type having a higher dopant concentration than that of the substrate and at the opposite face a second region of said second conductivity type having a higher dopant concentration than that of the substrate, wherein each of said faces has had removed from part of it by abrasion a depth of material which increases gradually as the outer edge is approached so that the junction between each of said regions and the substrate is exposed along a path following the shape of the perimeter of the slice but so that the removal of material ceases at a distance outwardly beyond the exposure of the junction to leave a rim of the original planar faces of the slice at its perimeter.

2. A slice according to claim 1, wherein the slice is a disc.

3. A slice according to claim 1, wherein the material of the slice is silicon.

4. A slice according to claim 1, wherein the edge of the slice is rounded in section.

5. A slice according to claim 1, wherein said first and second regions of said second conductivity type are formed by the diffusion of a dopant of said second conductivity type into the faces of the substrate so as to over-dope the original first conductivity type and form a junction therewith at a predetermined depth.

6. A slice according to claim 1, wherein said first and second regions of said second conductivity type extend around the outer edge of the slice to form a surface region which is broken only where each of said junctions is exposed.

7. A slice according to claim 1, wherein the gradual increase in depth of the removal of material constitutes an angle of less than 7° relative to the plane of the junction thereby exposed.

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8. A slice according to claim 7, wherein said angle is in the range from 2° to 5°.

9. A slice according to claim 7, wherein said angle is about 3°.

10. A slice according to claim 1, wherein the substrate material is of n-type conductivity and the surface regions are of p-type conductivity.

11. A slice according to claim 1 with the addition of further semiconductor regions and ohmically connected electrodes so as to form an operable electrical device.

12. A method of producing a semiconductor junction profile, comprising providing a planar slice of semiconductor substrate material of a first conductivity type provided at one face with a first region of a second conductivity type having a higher dopant concentration than that of the substrate and at the opposite face a second region of said second conductivity type, having a higher dopant concentration than that of the substrate, the method comprising removing from part of each of said faces by abrasion a depth of material which increases gradually as the outer edge is approached so that the junction between each of said regions and the substrate is exposed along a path following the shape of the perimeter of the slice but so that the removal of material ceases at a distance outwardly beyond the exposure of the junction to leave a rim of the original planar faces of the slice at its perimeter.

13. A method according to claim 12, wherein the slice is a disc.

14. A method according to claim 12, wherein the material of the slice is silicon.

15. A method according to claim 12, wherein the edge of the slice is rounded in section.

16. A method according to claim 12, wherein said first and second regions of said second conductivity type are formed by the diffusion of a dopant of said second conductivity type into the faces of the substrate so as to over-dope the original first conductivity type and form a junction therewith at a predetermined depth.

17. A method according to claim 12, wherein said first and second regions of said second conductivity type extend around the outer edge of the slice to form a surface region which is broken only where each of said junctions is exposed.

18. A method according to claim 12, wherein the gradual increase in depth of the removal of material constitutes an angle of less than 7° relative to the plane of the junction thereby exposed.

19. A method according to claim 18, wherein said angle is in the range from 2° to 5°.

20. A method according to claim 18, wherein said angle is about 3°.

21. A method according to claim 12, wherein the substrate material is of n-type conductivity and the surface regions are of p-type conductivity.